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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Katsumi Abe

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EXAMINER

PHAM, TAMMY T

ART UNIT

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2629

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DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/664,969	Applicant(s) ABE, KATSUMI	
	Examiner Tammy Pham	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 16-21 and 27-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 16-21 and 27-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Claims 1-7, 16-21, 27-32 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 May 2007 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 27, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over KUMADA et al. (US Application No: 2002/0008686 A1).

As for independent claims 1, KUMADA teaches of a common drive circuit (*Fig. 2, item 10 and Fig. 3*) for a display (*Fig. 2*), the common drive circuit (*Fig. 2, item 10 and Fig. 3*): comprising: a first voltage supply (*Fig. 3, item "positive power source"*) and a second voltage supply (*Fig. 3, item GND*) which respectively supply a high level voltage signal (*Fig. 3, item*

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Vdd) and a low level voltage signal (*Fig. 3, item GND*) to a common electrode (*Fig. 3, item "common electrode," section [0051]*); at least one first transistor (*Fig. 3, un-numbered item consisting of top transistor*) including either a drain or a source terminal connected to the first voltage supply (*Fig. 3, item "positive power source"*); at least one second transistor (*Fig. 3, un-numbered item consisting of bottom transistor*) including either a drain or source terminal connected to the second voltage supply (*Fig. 3, item GND*); at least one signal line (*Fig. 3, un-numbered item where V_{in} enters*) connected to each gate terminal of the first and second transistor (*Fig. 3, un-numbered item consisting of transistors, section [0050]*); and at least one capacitance load (*Fig. 3, item "to liquid crystal panel," and in Fig. 2, item 1*) connected to respective terminals of the first and the second transistors (*Fig. 3, un-numbered item consisting of transistors*) not connected to the first and second voltage supplies (*Fig. 3, items V_{dd} and GND , respectively, section [0043]*),

KUMADA fails to teach that the high level of a signal passing through at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and that the low level of the signal passing through the signal line is the same or lower than the low level voltage signal supplied by the second voltage supply.

Applicant has not disclosed any specific advantage or criticality to having the high level of a signal passing through be higher (and not the same as the voltage signal supplied by the first voltage supply); and similarly, Applicant has not disclosed any specific advantage or criticality to having the low level of a signal passing through be lower (and not the same as the voltage signal supplied by the second voltage supply). As such, the having the high and low level of the signal passing through be higher and lower, respectively, then the first and second supply voltage

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is an obvious matter of design choice. Further, as Applicant even states that the voltage of the signal passing through can be the same as the voltage supply (Specification, section [0019]).

It would have been obvious to one with ordinary skill in the art at the time the invention was made have the voltage of the signal passing through be the same as the supply voltage since (1) this aspects seems to allow the apparatus to function just as well as if the voltage of the signal passing through were higher or lower than the supply voltage; and (2) seems to simplify the circuitry since it allows the voltage from the voltage supply to pass through without any substantial modifications to the voltage levels.

As for claim 3, KUMADA teaches that the at least one first transistor (*Fig. 3, un-numbered item consisting of top transistor*) comprises P-type transistor and the at least one second transistors (*Fig. 3, un-numbered item consisting of bottom transistor*) comprises N-type transistor, and wherein the gate terminals of the first and second transistors (*Fig. 3, un-numbered item consisting of transistors*) are connected to common signal lines (*Fig. 3, item "common electrode signal"*) in section [0049]. (*NOTE: That KUMADA points that the Fig. 3 consists of C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS rae connected in parallel*).

As for claim 27, KUMADA teaches that the high level voltage signal (*Fig. 3, item Vdd*) supplied by the first voltage supply (*Fig. 3, item "positive power source"*) is a high level common voltage (VCOMH) (*Fig. 3, item Vdd*) and the low level voltage signal (*Fig. 3, item GND*) supplied by the second voltage supply (*Fig. 3, item GND*) is a low level common voltage

(VCOML) (Fig. 3, item GND), which are respectively supplied to the common electrode (VCOM) in Fig. 3 and in section [0050].

As for **claim 29**, KUMADA teaches of a level shift circuit (Fig. 2, item 20, section [0086]) connected to the one signal line (Fig. 2, item S(1-N)) directly.

4. Claims 2, 4-7, 16-21, 28, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over KUMADA et al. (US Application No: 2002/0008686 A1) in view of HOSOKAWA et al. (US Patent No: 4,393,380).

As for **independent claim 16**, KUMADA teaches of a display (Fig. 2) comprising: a substrate; a display portion (Fig. 2, item 1) integrated on the substrate (Fig. 2); and a gate driver circuit (Fig. 2, item 2), which controls switching of pixels (Fig. 2, item 7) of each line (Fig. 2, item G(1-M)) in a display portion (Fig. 2, item 1); a common drive circuit (Fig. 2, item 10) for the display portion (Fig. 2, item 1) for-which simultaneously driving capacitance loads (Fig. 2, item 1) in Fig. 2.

KUMADA fails to teach that the display portion (Fig. 2, item 1), wherein the common drive circuit (Fig. 2, item 10) is disposed on a position opposite to the gate driver circuit (Fig. 2, item 2) and the display portion (Fig. 2, item 1) therebetween.

HOKOKAWA teaches that the display portion (Fig. 4), wherein the common drive circuit (Fig. 4, items 3, 34) is disposed on a position opposite to the gate driver circuit (Fig. 4, item 2) and the display portion (Fig. 4, column 4, lines 29-32; lines 50-54) therebetween.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to take the display of KUMADA and rearrange the components so that the common drive circuit is opposite to the gate driver circuit and the display portion in between as taught by HOKOKAWA since it is well known that resistance is directly proportional to the length of wire. Hence, the shorter the wiring between two electrical components, the less resistance there is in transferring signals back and forth, and hence results in less driving time. Knowing this, it would have been obvious to position the common drive circuit as close to the reference voltage source as possible in order to reduce the driving time.

As for claim 2, as the limitations in claim 2 are similar to those in claim 16, claim 2 is rejected over the same merits as claim 16.

As for claim 17, KUMADA teaches of a common drive circuit (*Fig. 2, item 10 and Fig. 3*) for a display (*Fig. 2*), the common drive circuit (*Fig. 2, item 10 and Fig. 3*): comprising: a first voltage supply (*Fig. 3, item "positive power source"*) and a second voltage supply (*Fig. 3, item GND*) which respectively supply a high level voltage signal (*Fig. 3, item Vdd*) and a low level voltage signal (*Fig. 3, item GND*) to a common electrode (*Fig. 3, item "common electrode," section [0051]*); at least one first transistor (*Fig. 3, un-numbered item consisting of top transistor*) including either a drain or a source terminal connected to the first voltage supply (*Fig. 3, item "positive power source"*); at least one second transistor (*Fig. 3, un-numbered item consisting of bottom transistor*) including either a drain or source terminal connected to the second voltage supply (*Fig. 3, item GND*); at least one signal line (*Fig. 3, un-numbered item*

where *V_{in}* enters) connected to each gate terminal of the first and second transistor (Fig. 3, un-numbered item consisting of transistors, section [0050]); and at least one capacitance load (Fig. 3, item "to liquid crystal panel," and in Fig. 2, item 1) connected to respective terminals of the first and the second transistors (Fig. 3, un-numbered item consisting of transistors) not connected to the first and second voltage supplies (Fig. 3, items *V_{dd}* and *GND*, respectively, section [0043]), wherein a high level of a signal (Fig. 3, item *V_{dd}*) passing through the at least one signal line (Fig. 3, item *V_{in}*) is the same as the high level voltage signal (Fig. 3, item *V_{dd}*) supplied by the first voltage supply (Fig. 3, item "positive power source") and a low level (Fig. 3, item *GND*) of the signal passing through the signal line (Fig. 3, un-numbered item where *V_{in}* enters) is the same as the low level voltage signal (Fig. 3, item *GND*) supplied by the second voltage supply (Fig. 3, item *GND*) in section [0050].

As for claims 4, 19, KUMADA teaches that P-type transistors and N-type transistors are connected in parallel to be the first transistor (Fig. 3, un-numbered item consisting of the top transistor), and N-type transistors and P-type transistors are connected in parallel to be the second transistor (Fig. 3, un-numbered item consisting of the bottom transistor), wherein respective gates of the P-type transistors of the first transistor (Fig. 3, un-numbered item consisting of the top transistor) and the N-type transistor of the second transistors (Fig. 3, un-numbered item consisting of the bottom transistor) are connected to one the signal line (Fig. 3, un-numbered item in which *V_{in}* is coming in from), and respective gates of the N-type transistors of the first transistor (Fig. 3, un-numbered item consisting of the top transistor) and the P-type transistors of the second transistor (Fig. 3, un-numbered item consisting of the bottom

transistor) are connected to an inversion signal line (*NOTE: That since a C-MOS consist of a pair of p-type and n-type connected in parallel; the p-type is typically is active when the current is in an unconventional mode, in other words, can the p-type can be seen as connected to an inverted signal*) of one the signal line (Fig. 3, un-numbered item in which V_{in} is coming in from) in Fig. 3 and in section [0049]. (*NOTE: That KUMADA points that the Fig. 3 consists of C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS rae connected in parallel*).

As for claims 5, 20, KUMADA teaches that a high-level voltage (not shown) of each signal of the signal line (Fig. 2, items G(1-M)) and the inversion signal line (Fig. 6, item coming from 81) is a high-level line voltage (not shown) of the gate driver (Fig. 2, item 2) and wherein a low-level voltage (Fig. 3, item GND) of each signal of the signal line (Fig. 2, items G(I-M)) and the inversion signal line (Fig. 6, item coming from 81) is a low-level line voltage (not shown) of the gate driver (Fig. 2, item 2) in sections [0143, 0148]. (*NOTE: That section [0143] teaches that scan signals from the gate driver are used to adjust the voltage levels of all of the source signals supplied by the source driver for all pixels electrodes. All of the source signals includes signals such as V_{dd} from the positive power source in Fig. 3 that is considered to be the high-level voltage in the common driver of Fig. 3*).

As for claims 6, 21, KUMADA teaches that the first (Fig. 3, un-numbered item consisting of the top transistor) and second transistors (Fig. 3, un-numbered item consisting of the bottom transistor) are comprised of thin-film transistors in sections [0004-5].

As for claim 7, KUMADA teaches that the display portion comprises a liquid crystal display (Fig. 2) in section [0002].

As for claim 18, KUMADA teaches that the at least one first transistor (*Fig. 3, un-numbered item consisting of top transistor*) comprises P-type transistor and the at least one second transistors (*Fig. 3, un-numbered item consisting of bottom transistor*) comprises N-type transistor, and wherein the gate terminals of the first and second transistors (*Fig. 3, un-numbered item consisting of transistors*) are connected to common signal lines (Fig. 3, item “common electrode signal”) in section [0049]. (*NOTE: That KUMADA points that the Fig. 3 consists of C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS rae connected in parallel*).

As for claim 28, KUMADA teaches that the high level voltage signal (Fig. 3, item Vdd) supplied by the first voltage supply (Fig. 3, item “positive power source”) is a high level common voltage (VCOMH) (Fig. 3, item Vdd) and the low level voltage signal (Fig. 3, item GND) supplied by the second voltage supply (Fig. 3, item GND) is a low level common voltage (VCOML) (Fig. 3, item GND), which are respectively supplied to the common electrode (VCOM) in Fig. 3 and in section [0050].

As for claims 30-32, KUMADA teaches of a level shift circuit (not shown by taught in section [0134]) connected to the one signal line (not numbered but shown in Fig. 5, lines

connected to items 81, 82) directly and the inversion signal line (Fig. 6, items 81, 82, section [0131]).

Response to Arguments

5. Applicant's arguments with respect to claims 1-7, 16-21, 27-32 have been considered but are moot in view of the new ground(s) of rejection.

6. **In regards to claim 1**, Applicant argues that "*Kumada does not teach or suggest that Vin is higher than Vdd or lower than GND (Remarks 19-20).*" This argument is not persuasive.

Applicant does not list any advantages why the apparatus would prefer that Vin be of higher or lower value. Further, Applicant even teaches that Vin could be higher, lower or the same as the supplied voltages (section [0019]). This teachings implies that the main inventive concept of the apparatus is able to function irregardless if Vin is higher, lower or the same value as the supplied voltage.

7. **In regards to claim 16**, Applicant argues that "*Kumada does not disclose placing the common drive circuit opposite to the gate driver with the display portion in the middle (Remarks 20).*" This argument is not persuasive. Please look at the teachings of Hosokawa above for more reference.

8. **In regards to claims 4, 9**, Applicant argues that "*Kumada does not disclose ... N-type and P-type transistors in parallel (Remarks 23).*" This argument is not persuasive. Kumada teaches of a C-MOS, which is well known in the art to consist of a P and N type transistors.

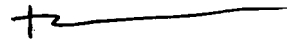
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
18 July 2007


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